USN | | | | | | | | | | |

08EC027

M.Tech. Degree Examination, December 2010
Design of VLSI System

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the structured strategies, used to reduce the complexity of design. **(08 Marks)**

b. Explain the design flow of automated layout generation. **(12 Marks)**

2 a. Compare the different VLSI design methods (Cell based, custom design & FPGA). **(07 Marks)**

b. Explain the programmed behavioral synthesis. **(07 Marks)**

c. What are gray cell and black cell? Explain. **(06 Marks)**

3 a. Explain the valency-4 Manchester carry chain, with a circuit diagram. Give the relevant equations. **(10 Marks)**

b. Explain the carry look ahead adder. Also, draw the group PG network for 16-bit CLA. **(10 Marks)**

4 a. Draw the table for radix 4 modified booth encoding values. Design a booth encoder and a booth selector, using this table. **(10 Marks)**

b. Explain and write the dot diagram for Wallace tree multiplier. **(06 Marks)**

c. Explain the prefix computation, with respect to priority encoder. **(04 Marks)**

5 a. Explain the read and write operation of 6T SRAM cell. **(08 Marks)**

b. Estimate the delays of 8:256 decoders, using static CMOS gates. Assume decoder has an electrical effort of H = 10 and that both complement and true inputs are available. **(06 Marks)**

c. Explain the advantages and disadvantages of NAND ROMs, as compared to NOR ROMs. **(06 Marks)**

6 a. Explain the bi-directional input-output pad circuitry. **(06 Marks)**

b. Define the clock skew, with an example. **(04 Marks)**

c. Give the classification of global clock distribution. Explain the H-trees for global clock distribution. **(10 Marks)**

7 a. Explain the non-recurring engineering costs and recurring costs, in the design economics. **(08 Marks)**

b. Explain the various levels of logic verification. **(08 Marks)**

c. What is a test bench? How is it used to verify the design? **(04 Marks)**

8 a. Explain the following :

i) Observability and controllability

ii) Stuck-At-0 and Stuck-At-1 **(08 Marks)**

b. How is the pseudo random sequence generator used, in the built-in-self-test design? **(06 Marks)**

c. With a neat diagram, explain the boundary scan architecture. **(06 Marks)**

* * * * *

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.